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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/675,974
Filing Date: September 29, 2000
Appellant(s): BOWLIN, STAN W

James H. Walters (Reg. No. 35,731)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 14th of July 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying no related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 12th of December 2003 has not been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The summary of invention contained in the brief is deficient because the Appellant's statement is not fully supported by the specification.

The Appellant's statement in the brief, on page 5, lines 1-4, i.e., the various operations from time 1 to 6/7 are done to set the operation up and at time T6/7-T13, the MAC data on signal 34 is thereby substantially simultaneously supplied to the SDRAM and to the DSP, is not disclosed in the specification.

In contrary to the Appellant's statement, the specification discloses that the various operations from time 1 to 6/7 (i.e., DSP_Command 26 is set ACTIVE at T1/2, READ at T4/5, and SDRAM_Command 30 is set ACTIVE at T2, WRITE at T7 in Fig. 2) are done to set up the read operation by DSP_Command at T4/5, and set up the write operation by SDRAM_Command at T7, and continuously, at time T6/7-T13, the MAC data on signal 34 is thereby supplied to the SDRAM and to the DSP with the 2 cycle time latency (i.e., difference) between the reading and writing operations. In other words, a data W (e.g., W3) on RX_Data at a specific cycle time (i.e., T9) is written into SDRAM at said specific cycle time, but said

data W (i.e., W3) is not read by DSP_Command at said specific cycle time because the reading operation was commanded (i.e., read) 2 clock cycles before said specific cycle time. In order to substantially simultaneously supply a MAC data on RX_Data to the SDRAM and to the DSP, the DSP_Command is set READ at a specific cycle time, and at the same time, SDRAM_Command is set WRITE at said specific cycle time (i.e., overlapped operation), which has never been disclosed in the specification. Therefore, the statement in the Summary of Invention, i.e., the various operations from time 1 to 6/7 are done to set the operation up and at time T6/7-T13, the MAC data on signal 34 is thereby substantially simultaneously supplied to the SDRAM and to the DSP, is deficient because the MAC data on signal 34 is not substantially simultaneously supplied to the SDRAM and to the DSP, but the MAC data on signal 34 is supplied to the SDRAM by SDRAM_Command 'WRITE' at a specific cycle time, and another MAC data on signal 34 is supplied to the DSP by DSP_Command 'READ' at 2 cycles later after said specific cycle time.

(7) Grouping of Claims

Appellant states that the claims 1-9 and 12-19 may be considered to stand or fall together, but the claims 1-9 and 12-19 do not stand or fall together with the claims 10 and 11, and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

US 5,073,851	Masterson et al.	12-1991
US 5,379,289 A	DeSouza et al.	1-1995

Applicant Admitted Prior Art - Specification page 2, line 34 through page 3, line 4

IBM TDB "Circuit for Tracing Branch Instructions" by IBM Technical Disclosure Bulletin, Vol. 22, no. 7 (Dec. 1979), pp2651-2654

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-19 are rejected under 35 U.S.C. 112, first paragraph

Regarding to claims 1, 8, 9 and 16, the specification, while being enabling for transferring a first word (e.g., W3 at cycle 9 in Fig. 2) of RX_Data 34 (Fig. 2) on BUS 16 (Fig. 1) from MAC FIFO 14 (Fig. 1) to SDRAM 18 (Fig. 1) and DSP 20 (Fig. 1), i.e., supplying a second word of data (i.e., W5 at cycle 9) from the MAC FIFO to DSP as a read data operation even though the data W5 is not available on RX_Data 34 at cycle 9 (i.e., reading W5 at cycle 9 in Fig. 2 because of 2 clock cycles latency), and supplying said first word of data (i.e., W3) to SDRAM as a write data operation (i.e., writable W3 at cycle 9 in Fig. 2 because RX_Data has W3 at cycle 9; See Timing flow chart in Fig. 2), does not reasonably provide enablement for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, i.e., supplying said unit of data from the source to first of said at least two destinations as a read data operation, and supplying said unit of data to a second of said at least two destinations as a write data operation, which is shown in claim 1 as an exemplary claim. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

The Examiner doubts how to transfer a unit of data on a bus from a source to at least two destinations substantially simultaneously at a specific cycle time because the Appellant admits that there are 2 clock cycles latency between a read data operation and a write data operation (i.e., no operation cycle overlapping between the reading cycle for a data from MAC and writing cycle for said data into SDRAM; See Fig. 2 and page 4, lines 23-24). In other words, at a specific cycle time T9, the data W3 is available on RX_Data, and it could be written into SDRAM. However, at said specific cycle time T9, DSP does not

read the data W3, but read the data W5 at said specific cycle time T9, which will be available at 2 cycle times later on the RX_Data.

Therefore, the Examiner assumes that the subject matter "a unit of data" or the like for a read operation is different from the subject matter "a unit of data" or the like for a write operation if both of the operations are performed substantially simultaneously for the claim rejection based on prior art.

The Claims 2-7, 12, 13, 18 and 19 are dependent claims of the claim 1.

The Claims 14 and 15 are dependent claims of the claim 8.

The Claims 10 and 11 are dependent claims of the claim 9.

The Claim 17 is a dependent claim of the claim 16.

Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph

Regarding to claims 10 and 11, the claims are respectively indefinite for failing to particularly point out and distinctly claim the subject matter which appellant regards as the invention.

The claims recite respectively the limitation "said FIFO device" in line 1 of the claim 10, and in line 3 of the claim 11. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "said FIFO device" could be considered as --said FIFO data source-- since it is not clearly defined in the claims, and for the claim rejection based on prior art.

Claims 1, 4-8, 12, 14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Masterson et al. [US 5,073,851; hereinafter Masterson].

Fact findings for Claim 1

Claimed Elements	AAPA's Facts
a) a method for transferring a first unit of data on a bus from a source to at least two destinations	a) a method for transferring a first unit of data (e.g., byte or word depending on the read/write operation boundary alignment) on a bus from a

	source, i.e., MAC to at least two destinations, i.e., DSP and SDRAM (See page 2, line 34 through page 3, line 4)
b) supplying a second unit of data from said source to first of said at least two destinations as a read data operation	b) supplying a second unit of data from said source, i.e., MAC, to said DSP as a read data operation (See page 2, line 35)
c) supplying said first unit of data to a second of said at least two destinations as a write operation	c) supplying said first unit of data to said SDRAM as a write operation (See page 3, line 2)
	Masterson's Facts
d) a first and second units of data transferring would been substantially simultaneously performed	d) a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1) (See Claim 1 and col. 5, lines 57-60)

Referring to claim 1, AAPA discloses a method for transferring a first unit of data (e.g., byte or word depending on the read/write operation boundary alignment) on a bus (See page 2, line 34 through page 3, line 4) from a source (i.e., MAC) to at least two destinations (i.e., DSP and SDRAM), comprising the steps of: supplying a second unit of data from said source (i.e., MAC) to first of said at least two destinations (i.e., DSP) as a read data operation (See page 2, line 35); and supplying said first unit of data to a second of said at least two destinations (i.e., SDRAM) as a write operation (See page 3, line 2). AAPA does not teach said first and second units of data transferring would been substantially simultaneously performed.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a first and second units of data transferring would been substantially simultaneously performed (See claim 1 and col. 5, lines 57-60; i.e., a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of data transferring control (i.e., by the timing controller in gate array), as disclosed by Masterson, in said method of data transferring, as disclosed by AAPA, so as to pass said unit of data (i.e., byte 1, byte 2, byte 3, ... etc.) to said one of at least two destinations as a read

operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation), which is disclosed at Masterson, col. 3, lines 60-65.

Fact findings for Claims 4-7

Claimed Elements	AAPA's Facts
a) at least one of said at least two destinations comprise addressed data devices	a) at least one of said at least two destinations, i.e., SDRAM and DSP, comprise addressed data devices, i.e., SDRAM is a synchronous dynamic random access memory, which is accessed through an address bus, and DSP is a digital signal processor, which is accessing an external data through said address bus, too.
b) the at least one destinations comprises a microprocessor	b) said DSP comprising a microprocessor, i.e., DSP stands for Digital Signal Processor.
c) the at least one destinations comprises a memory storage, which is SDRAM	c) said SDRAM comprising a memory storage, which stands for Synchronous Dynamic Random Access Memory

Referring to claim 4, AAPA teaches that at least one of said at least two destinations (i.e., SDRAM and DSP) comprise addressed data devices (i.e., SDRAM is a synchronous dynamic random access memory, which is accessed through an address bus, and DSP is a digital signal processor, which is accessing an external data through said address bus, too).

Referring to claim 5, AAPA teaches said at least one destinations comprises a microprocessor (i.e., DSP stands for Digital Signal Processor).

Referring to claims 6 and 7, AAPA teaches said at least one destinations comprises a memory storage, which is SDRAM (i.e., SDRAM stands for Synchronous Dynamic Random Access Memory).

Fact findings for Claim 8

Claimed Elements	AAPA's Facts
a) an apparatus for transferring received data in discrete units from a network	a) an apparatus, i.e., network test device, for transferring received data in discrete units from a network (See page 2, line 34 through page 3, line 4)

b) a bus	b) a bus (See page 3, line 1)
c) a media access controller for putting ones of discrete units of the received data from the network onto said bus	c) a media access controller, i.e., MAC in page 2, line 35, for putting ones of discrete units of said received data from said network onto said bus (See page 2, lines 34-35)
d) a microprocessor for reading the ones of discrete units of data from said bus	d) a DSP for reading said ones of discrete units of data from said bus (See page 2, line 35)
e) a memory for writing the ones of discrete units of data from said bus into said memory	e) an SDRAM for writing said ones of discrete units of data from said bus into said SDRAM (See page 3, line 2)
	Masterson's Facts
f) a timing controller for controlling said media access controller	f) a gate array 34 (i.e., timing controller) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) main memory 15 in Fig. 2 (i.e., a media access controller)
g) said microprocessor and said memory to have said media access controller write a first selected ones of discrete units of said data to the bus	g) CPU 12 (i.e., microprocessor) and a cache 18 (i.e., memory) in Fig. 2 to have said main memory (i.e., media access controller) write a first selected ones of discrete units of said data (e.g., byte 1) to a bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said media access controller (i.e., main memory) write data to a bus)
h) said memory write said first selected ones of discrete units of the data to said memory and said microprocessor read a second selected ones of discrete units of the data substantially simultaneously	h) said cache (i.e., memory) write said first selected ones of discrete units of said data (i.e., byte 1) to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said CPU (i.e., microprocessor) read a second selected ones of discrete units of said data (i.e., byte 2 read access of the main memory, furnished by CPU) substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68)

Referring to claim 8, AAPA discloses an apparatus (i.e., network test device) for transferring received data in discrete units from a network (See page 2, line 34 through page 3, line 4), comprising: a bus (See page 3, line 1); a media access controller (i.e., MAC in page 2, line 35) for putting ones of discrete units of said received data from said network onto said bus (See page 2, lines 34-35); a microprocessor (i.e., DSP) for reading said ones of discrete units of data from said bus (See page 2, line

35); a memory (i.e., SDRAM) for writing said ones of discrete units of data from said bus into said memory (See page 3, line 2).

AAPA does not disclose a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write a first selected ones of discrete units of said data to said bus, said memory write said first selected ones of discrete units of said data to said memory and said microprocessor read a second selected ones of discrete units of said data substantially simultaneously.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a timing controller (i.e., gate array 34 of Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) a media access controller (i.e., main memory 15 of Fig. 2), a microprocessor (CPU 12 of Fig. 2) and a memory (i.e., cache 18 of Fig. 2) to have said media access controller (i.e., main memory) write a first selected ones of discrete units of said data (e.g., byte 1) to a bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said media access controller (i.e., main memory) write data to a bus), said memory (i.e., cache) write said first selected ones of discrete units of said data (i.e., byte 1) to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said microprocessor (i.e., CPU) read a second selected ones of discrete units of said data (i.e., byte 2 read access of the main memory, furnished by CPU) substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said timing controller, as disclosed by Masterson, in said apparatus, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage

of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation), which is taught by Masterson at col. 3, lines 60-65.

Fact findings for Claim 12

Claimed Elements	Masterson's Facts
a) said supplying as a read and write operation of said units of data is accomplished with said units of data being presented on said bus as a single instance	a) said supplying as a read and write operation of said units of data (i.e., byte 1, byte 2, byte 3, ... etc.) is accomplished with said units of data being presented on said bus as a single instance (i.e., byte)

Referring to claim 12, Masterson teaches said supplying as a read and write operation of said units of data (i.e., byte 1, byte 2, byte 3, ... etc.) is accomplished with said units of data being presented on said bus as a single instance (i.e., byte).

Fact findings for Claim 14

Claimed Elements	AAPA's Facts
a) said apparatus comprises a network test instrument·	a) said apparatus comprises a network test device (i.e., network test instrument; See page 2, lines 27, 28, and line 34 through page 3, line 3)

Referring to claim 14, AAPA teaches said apparatus comprises a network test instrument (i.e., network test device; See page 2, lines 27, 28, and line 34 through page 3, line 3).

Fact findings for Claim 15

Claimed Elements	Masterson's Facts
a) said memory write of said first selected quantity of data to said memory and said microprocessor read of the second selected quantity of data are accomplished with said first and second selected quantity of data being presented on said bus as a single instance	a) said cache (i.e., memory) write of said first selected quantity of data (i.e., byte 1) to said memory and said microprocessor read of said second selected quantity of data (i.e., byte 2) are accomplished with said first and second selected quantity of data being presented on said bus as a single instance (i.e., byte)

Referring to claim 15, Masterson teaches said memory (i.e., cache 18 of Fig. 2) write of said first selected quantity of data (i.e., byte 1) to said memory and said microprocessor read of said second selected quantity of data (i.e., byte 2) are accomplished with said first and second selected quantity of data being presented on said bus as a single instance (i.e., byte).

Fact findings for Claim 16

Claimed Elements	AAPA's Facts
a) a method for operating a network test instrument to transfer data on a bus within said network test instrument from a media access controller at least to a processor and to a memory, separate from said processor	a) a method for operating a network test device (i.e., network test instrument; See page 2, lines 27, 28, and line 34 through page 3, line 3) to transfer data, i.e., data in byte or word depending on the read/write operation boundary alignment, on a bus within said network test device (See page 2, line 34 through page 3, line 4) from an MAC at least to a DSP (i.e., processor) and to a memory, separate from said CPU (i.e., SDRAM)
b) supplying said data from said media access controller to said processor as a read data operation performed by said processor	b) supplying said data from said MAC to said DSP as a read data operation performed by said DSP (i.e., processor; See page 2, line 35)
c) supplying said data to said memory as a write operation	c) supplying said data to said SDRAM as a write operation (See page 3, line 2)
	Masterson's Facts
d) supplying data to said processor and supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus	d) supplying data (e.g., byte 2 of data) to a CPU 12 (i.e., processor) and supplying data (i.e., byte 1 of data) to a cache 18 (i.e., memory) in Fig. 2 are accomplished substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68) with use of the same transfer (i.e., overlapped transferring operation) of said data (i.e., said byte 1 and 2 are included in said data) on a bus (See claim 1 and col. 5, lines 57-60; i.e., a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1))

Referring to claim 16, AAPA discloses a method for operating a network test instrument (i.e., network test device; See page 2, lines 27, 28, and line 34 through page 3, line 3) to transfer data (i.e., data in byte or word depending on the read/write operation boundary alignment) on a bus within said network

test instrument (See page 2, line 34 through page 3, line 4) from a media access controller (i.e., MAC) at least to a processor (i.e., DSP) and to a memory, separate from said processor (i.e., SDRAM), comprising the steps of : supplying said data from said media access controller (i.e., MAC) to said processor (i.e., DSP) as a read data operation performed by said processor (See page 2, line 35); and supplying said data to said memory (i.e., SDRAM) as a write operation (See page 3, line 2).

AAPA does not teach said step of supplying data to said processor and said step of supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein step of supplying data (e.g., byte 2 of data) to a processor (i.e., CPU 12 of Fig. 2) and step of supplying data (i.e., byte 1 of data) to a memory (i.e., cache 18 of Fig. 2) are accomplished substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68) with use of the same transfer (i.e., overlapped transferring operation) of said data (i.e., said byte 1 and 2 are included in said data) on a bus (See claim 1 and col. 5, lines 57-60; i.e., a read operation of a first unit of data (e.g., byte 2) is substantially simultaneously overlapped with a write operation of a second unit of data (i.e., byte 1)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of data transferring control (i.e., by the timing controller in gate array), as disclosed by Masterson, in said method of data transferring, as disclosed by AAPA, so as to pass said data (i.e., byte 1, byte 2, byte 3, ... etc.) to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation), which is disclosed at Masterson, col. 3, lines 60-65.

Referring to claim 19, AAPA, as modified by Masterson, does not expressly teach said units of data comprises a word.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said units of data in word boundary alignment, such that said memory read/write operation and bus operation are based on said word boundary alignment, since it was well known in the art that a memory access and bus operations in word boundary alignment is faster than a memory access and bus operation in byte boundary alignment.

Furthermore, it would have been an obvious matter of design choice to use said units of data in word, since the Appellant has not disclosed that said units of data in word solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with AAPA, as modified by Masterson. In other words, the limitation in the claim, i.e., "said units of data comprising a word", is recited without any patentable advantage in the specification.

Therefore, the claimed limitation "said units of data comprising a word" is not patentably significant since it at most relates to the size of the claimed subject matter "unit of data" under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Claims 2, 3, 9-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Masterson [US 5,073,851] as applied to claims 1, 4-8, 12, 14-16 and 19 above, and further in view of DeSouza et al. [US 5,379,289 A; hereinafter DeSouza].

Fact findings for Claims 2 and 3

Claimed Elements	DeSouza's Facts
a) said source comprises a non-addressed data device	a) a media access controller (i.e., source) comprising a receiver FIFO 20 in Fig. 6 (i.e., non-addressed data device; See col. 2, lines 5-14, wherein in fact that the data stored in the receiver FIFO is then transferred to a user system implies that said source (i.e., media access controller) comprises a receiver FIFO,

	which is a non-addressed data device since said stored data is transferred to said user system without being accessed by said user system)
b) the source comprises a FIFO device	b) said source comprising a receiver FIFO 20 in Fig. 6 (i.e., FIFO device)

Referring to claim 2, AAPA, as modified by Masterson, discloses all the limitations of the claim 2 except that does not teach said source comprises a non-addressed data device.

DeSouza discloses a media access controller (See Abstract and Fig. 6), wherein a source (i.e., media access controller in Fig. 6) comprises a non-addressed data device (i.e., receiver FIFO 20 of Fig. 6; See col. 2, lines 5-14, wherein in fact that the data stored in the receiver FIFO is then transferred to a user system implies that said source (i.e., media access controller) comprises a receiver FIFO, which is a non-addressed data device since said stored data is transferred to said user system without being accessed by said user system).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said receiver FIFO, as disclosed by DeSouza, in said source (i.e., MCA), as disclosed by AAPA, as modified by Masterson, so as to transfer incoming data stream to said destinations (e.g., memory and processor) in succession (i.e., first-in-first-out sequence) with the advantage of providing a buffering function, which is well known to one of ordinary skill in the art of digital circuit design.

Referring to claim 3, DeSouza teaches said source comprises a FIFO device (i.e., receiver FIFO 20 of Fig. 6).

Fact findings for Claim 9

Claimed Elements	AAPA's Facts
a) an apparatus for transferring data	a) an apparatus, i.e., network test device, for transferring data (See page 2, line 34 through page 3, line 4)
b) a bus	b) a bus (See page 3, line 1)
c) a data source connected to said bus for putting data onto said bus	c) a data source, i.e., MAC in page 2, line 35, connected to said bus for putting data onto said

	bus (See page 2, lines 34-35)
d) a microprocessor connected to said bus for reading said data from said bus	d) a DSP (i.e., microprocessor) connected to said bus for reading said data from said bus (See page 2, line 35)
e) a memory connected to said bus for writing said data from said bus into said memory	e) an SDRAM (i.e., memory) connected to said bus for writing said data from said bus into said memory (See page 3, line 2)
	Masterson's Facts
f) a timing controller connected to said data source, said microprocessor and said memory for controlling said data source	f) a gate array 34 (i.e., timing controller) connected to a main memory 15 (i.e., data source; i.e., the gate array 34 is connected to the main memory 15 via the main memory control line and the main memory address line), a microprocessor (i.e., the gate array 34 is connected to the CPU 12 via the control lines) and a memory (i.e., cache 18; i.e., the gate array 34 is connected to the cache 18 via the cache memory control line and the cache address line, shown in Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) said data source, i.e., main memory 15, shown in Fig. 2
g) said microprocessor and said memory to have said data source put said data onto said bus	g) said CPU 12 (i.e., microprocessor) and said cache 18 (i.e., memory) to have said data source (i.e., main memory) put said data onto said bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said data source (i.e., main memory) put data to said bus), shown in Fig. 2
h) said microprocessor and said memory, for a selected quantity of data, to have said memory write said selected quantity of data to said memory and said microprocessor read said selected quantity of data substantially simultaneously	h) said CPU 12 (i.e., microprocessor) and said cache 18 (i.e., memory), and for a selected quantity of data (i.e., data, which consists of byte 1, byte 2, byte 3, ... etc.), to have said cache (i.e., memory) write said selected quantity of data to said memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said CPU (i.e., microprocessor) read said selected quantity of data (i.e., read access of the main memory, furnished by CPU; See col. 5, lines 58-59) substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68), shown in Fig 2
	DeSouza's Facts
i) said data source is a FIFO data source	i) a media access controller (i.e., data source) comprising a receiver FIFO 20 in Fig. 6 (i.e., FIFO data source)

Referring to claim 9, AAPA discloses an apparatus (i.e., network test device) for transferring data (See page 2, line 34 through page 3, line 4), comprising: a bus (See page 3, line 1); a data source (i.e., MAC in page 2, line 35) connected to said bus for putting data onto said bus (See page 2, lines 34-35); a microprocessor (i.e., DSP) connected to said bus for reading said data from said bus (See page 2, line 35); a memory (i.e., SDRAM) connected to said bus for writing said data from said bus into said memory (See page 3, line 2).

AAPA does not disclose a timing controller connected to said data source, said microprocessor and said memory for controlling said data source, said microprocessor and said memory to have said data source put said data onto said bus, and for a selected quantity of data, have said memory write said selected quantity of data to said memory and said microprocessor read said selected quantity of data substantially simultaneously.

Masterson discloses an apparatus and method for improved caching in a computer system, wherein a timing controller (i.e., gate array 34 of Fig. 2) connected to a data source (i.e., the gate array 34 is connected to the main memory 15 via the main memory control line and the main memory address line, shown in Fig. 2), a microprocessor (i.e., the gate array 34 is connected to the CPU 12 via the control lines, shown in Fig. 2) and a memory (i.e., the gate array 34 is connected to the cache 18 via the cache memory control line and the cache address line, shown in Fig. 2) for controlling (i.e., through cache memory control, main memory control and control lines from CPU in Fig. 2) said data source (i.e., main memory 15 of Fig. 2), said microprocessor (i.e., CPU 12 of Fig. 2) and said memory (i.e., cache 18 of Fig. 2) to have said data source (i.e., main memory) put said data onto said bus (See col. 5, lines 45-54; i.e., wherein in fact that the DRAM controller provides an output enable signal to the main memory, then information in the main memory is accessed using addresses furnished by CPU implies that said data source (i.e., main memory) put data to said bus), and for a selected quantity of data (i.e., data, which consists of byte 1, byte 2, byte 3, ... etc.), have said memory (i.e., cache) write said selected quantity of data to said

memory (i.e., write access of the cache memory; See col. 5, lines 59-60) and said microprocessor (i.e., CPU) read said selected quantity of data (i.e., read access of the main memory, furnished by CPU; See col. 5, lines 58-59) substantially simultaneously (i.e., reading access of main memory and writing access of cache memory are substantially simultaneously overlapped; See col. 5, lines 37-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said timing controller, as disclosed by Masterson, in said apparatus, as disclosed by AAPA, so as to pass said data to said one of at least two destinations as a read operation, and to said other one of at least two destinations as a write operation substantially simultaneously with the advantage of speeding said operation of said transferring large amount of data (i.e., large blocks of information) during receiving data (i.e., during cache fill operation). Refer to Masterson, col. 3, lines 60-65.

AAPA, as modified by Masterson, does not expressly teach said data source is a FIFO data source.

DeSouza discloses a data source (i.e., media access controller in Fig. 6) comprises a FIFO data source (i.e., receiver FIFO 20 of Fig. 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said receiver FIFO, as disclosed by DeSouza, in said data source (i.e., MCA), as disclosed by AAPA, as modified by Masterson, so as to transfer incoming data stream to said destinations (e.g., memory and processor) in succession (i.e., first-in-first-out sequence) with the advantage of providing a buffering function, which is well known to one of ordinary skill in the art of digital circuit design.

Fact findings for Claims 10, 11 and 13

Claimed Elements	AAPA's Facts
a) said data source is a media access controller	a) said data source (i.e., MAC in page 2, line 35) is a media access controller
	DeSouza's Facts
b) said data source including FIFO receiver	b) said data source (AAPA, as modified by Masterson) including FIFO receiver (i.e., FIFO data source; DeSouza)

Referring to claim 10, AAPA, as modified by Masterson and DeSouza, teaches said data source (i.e., MAC in page 2, line 35; AAPA) including FIFO receiver (i.e., FIFO data source; AAPA, as modified by Masterson and DeSouza) is a media access controller (i.e., MAC).

Referring to claim 11, AAPA, as modified by Masterson and DeSouza, teaches said apparatus is a network test instrument, which is taught by AAPA at page 2, lines 27, 28, and line 34 through page 3, line 3, and said data source (i.e., MAC in page 2, line 35; AAPA) including FIFO receiver (i.e., FIFO data source; AAPA, as modified by Masterson and DeSouza) is a media access controller (i.e., MAC).

Referring to claim 13, AAPA, as modified by Masterson and DeSouza, teaches said source (i.e., MAC in page 2, line 35; AAPA) including FIFO receiver (i.e., FIFO data source; AAPA, as modified by Masterson and DeSouza) is a media access controller (i.e., MAC).

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Masterson [US 5,073,851] as applied to claims 1, 4-8, 12, 14-16 and 19 above, and further in view of IBM_TDB ["Circuit for Tracing Branch Instructions" by IBM Technical Disclosure Bulletin, December 1979, Vol. 22, Issue No. 7, pages 2651-2654].

Fact findings for Claims 17 and 18

Claimed Elements	IBM_TDB's Facts
a) determining whether said data, which is said unit of data, currently transferred to said memory, which is SDRAM, is to be retained before a next data (i.e., a next unit of data), is transferred said memory, and if said data currently transferred is to be retained, modifying a next write address location so that a next data does not overwrite said data currently transferred, and otherwise, if said data currently transferred is not to be retained in said memory, keeping said next data write address as a current data write address value so that said next data is written over said data currently transferred	a) determining (i.e., by Branch Detect Circuit in Fig. 1) whether an instruction (i.e., data) currently transferred to a Trace Memory in Fig. 1 (i.e., memory) is to be retained before a next data is transferred said Trace Memory (See Disclosure Text, 2nd paragraph, lines 1-4), and if said instruction currently transferred is to be retained (i.e., if the current instruction is a branch instruction), modifying a next write address location so that a next instruction does not overwrite said instruction currently transferred (See Disclosure Text, 2nd paragraph, lines 8-14 and 17-19), and otherwise, if said instruction currently transferred is not to be retained in said Trace Memory, keeping said next instruction write address as a current

	instruction write address value so that said next instruction is written over said instruction currently transferred (See Disclosure Text, 2nd paragraph, lines 6-8 and 15-16)

Referring to claims 17 and 18, AAPA, as modified by Masterson, discloses all the limitations of the claims 17 and 18, respectively, except that does not teach determining whether said data, which is said unit of data, currently transferred to said memory, which is SDRAM, is to be retained before a next data (i.e., a next unit of data), is transferred said memory, and if said data currently transferred is to be retained, modifying a next write address location so that a next data does not overwrite said data currently transferred, and otherwise, if said data currently transferred is not to be retained in said memory, keeping said next data write address as a current data write address value so that said next data is written over said data currently transferred.

IBM_TDB discloses a tracing test system, wherein determining (i.e., by Branch Detect Circuit in Fig. 1) whether a data (i.e., instruction) currently transferred to a memory (i.e., Trace Memory in Fig. 1) is to be retained before a next data is transferred said memory (See Disclosure Text, 2nd paragraph, lines 1-4), and if said data currently transferred is to be retained (i.e., if the current instruction is a branch instruction), modifying a next write address location so that a next data does not overwrite said data currently transferred (See Disclosure Text, 2nd paragraph, lines 8-14 and 17-19), and otherwise, if said data currently transferred is not to be retained in said memory, keeping said next data write address as a current data write address value so that said next data is written over said data currently transferred (See Disclosure Text, 2nd paragraph, lines 6-8 and 15-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method steps of tracing test system, as disclosed by IBM_TDB, in said method, as disclosed by AAPA, as modified by Masterson, so as to record said data (i.e., each instruction) operated on a network (i.e., executed by a processor) under test, for the advantage of generating an audit trail that is helpful in system debug (See Disclosure Text, 1st paragraph, lines 1-3).

(11) Response to Argument

In response to the Appellant's argument with respect to "... The Examiner says that applicant admits in the specification that there is a 2 cycle delay in a read operation and that therefore the transfer to at least two destinations substantially simultaneously is not enabled. Applicant disagrees. ... The RX_Data 34 appears on the bus for reading by the DSP and writing to the memory storage only at the timing shown. That is, at cycle 9, for example, data W3 is present on the bus. That is the only time that the transfer from the bus to both the DSP and the memory device can be effected for a specific data unit (W3, in the example discussed herein). The data cannot start being read by the DSP from the bus before it appears on the bus. Similarly, the data cannot be read after it is no longer on the bus. ..." on Brief page 7, lines 4-19, the Examiner respectfully disagrees.

In fact, the Appellant recites the limitation "transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously" in the claim. However, the specification discloses that transferring a first word (e.g., W3 in Fig. 2) of RX_Data 34 (Fig. 2) on BUS 16 (Fig. 1) from MAC FIFO 14 (Fig. 1) to SDRAM 18 (Fig. 1) at T9, and transferring a second word (i.e., W5 in Fig. 2) of RX_Data 34 (Fig. 2) on BUS 16 (Fig. 1) from MAC FIFO 14 (Fig. 1) to DSP 20 (Fig. 1) at T9, i.e., transferring said second word of data (i.e., W5) from the MAC FIFO to DSP during T7-8 as a read data operation even though the data W5 has not been available on RX_Data 34 at T9 because of 2 clock cycles latency (i.e., reading W5 at T9 in Fig. 2, which means the claimed subject matter "transferring" starts at T9), and transferring said first word of data (i.e., W3) to SDRAM as a write data operation (i.e., writable W3 at T9 in Fig. 2 because RX_Data has.W3 at T9; See Timing flow chart in Fig. 2). Therefore, the specification discloses "transferring a unit of data on a bus from a source to at least two destinations" is not performed substantially simultaneously. In other words, a unit of data (e.g., W3) is transferred to DSP at T6/7-9 by a read data operation, and said unit of data (i.e., W3) is transferred to SDRAM at T9 by a write data operation.

Thus, the specification does not reasonably provide enablement for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, i.e., supplying said unit of data from the source to first of said at least two destinations as a read data operation, and supplying said unit of data to a second of said at least two destinations as a write data operation, which is shown in claim 1 as an exemplary claim.

Furthermore, the Appellant assets the data cannot start being read by the DSP from the bus before it appears on the bus. However, the claim recites the data transferring from a data source (i.e., not a bus) to at least two destinations substantially simultaneously, and then the data should start being read by the DSP from the data source before it appears on the bus.

Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

In response to the Appellant's argument with respect to "The data is present for a set period of time (typically one clock cycle, but in the case of W1, it is 2 clock cycles in the particular embodiment illustrated) and during that time transfer to the first data source as a read and to the second data source as a write are effected. Merely because the timing of operation of one device in the illustrated example requires a read signal to be enabled before the read data is present does not make the specification non-enabling. It only shows the timing required for supplying signals to the various devices to get them to behave in the manner applicant desires in this embodiment." on Brief page 7, line 20 through page 8, line 5, the Examiner believes that the Appellant misunderstands the claim rejection.

Actually, the Examiner states Claims 1-19 rejection under 35 U.S.C. 112, first paragraph (scope enablement issue), i.e., the specification does not reasonably provide enablement for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, because the Appellant's specification could not make the scope of the claimed invention enable.

Furthermore, it is noted that the features upon which appellant relies (i.e., the data is present for a set period of time and during that time transfer to the first data source as a read and to the second data source as a write are effected) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to "Further, ... first, row address data is supplied to the memory device, then, 2 clock cycles later, a READ signal is supplied on the DSP device command signal line and the column selection signal COL is supplied to the memory device. This does not state that a 2 cycle latency is present between a read and a write. It merely teaches the timing of the control signals to effect the various devices to properly access the data in the RX_Data bus during the short time that each data Wl, W2, W3, etc., is present." on Brief page 8, lines 6-16, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, i.e., a 2 cycle latency is not present between a read and a write, it is clearly disclosed in the specification (See Fig. 2), such that DSP Command 26 is set ACTIVE at T1/2, READ at T4/5, and SDRAM_Command 30 is set ACTIVE at T2, WRITE at T7 in Fig. 2. Further, DSP Command 26 is set STOP at T11/12 2 cycles before SDRAM_Command 30 is set STOP at T14 in Fig. 2. It clearly shows that a 2 cycle latency is present between said read and said write operations because the actual read and write operations are not overlapped, which means said read and said write operations (i.e., data transferring) could not be substantially simultaneously performed.

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to "Paraphrasing what the Examiner says, he seems to be looking at the timing chart of FIG. 2 and say that the write command at time T7 is the 'write operation' and so that the data on the received data line at time T9 has already been written at time

T7. This interpretation is not correct and would not be possible in a world such as ours where time is linear. ..." on Brief page 8, line 17 through page 9, line 14, the Examiner believes that the Appellant wrongly paraphrases the Examiner's claim rejection.

In contrary to the Appellant's allegation, the Examiner has never stated the above alleged issues. Furthermore, the Appellant fails to provide any evident portion of the Examiner's statements in the record at where the above alleged issues were stated.

Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

In response to the Appellant's argument with respect to " The Examiner says that applicant admits that there are 2 clock cycles latency between a read data operation and a write data operation (referring to page 4, lines 23-24). This is not at all what applicant is stating. Applicant is merely discussing in that portion of the specification the specific timing of a disclosed embodiment of the invention is setting up the various chips in order to have the invention be accomplished, and in that case, setting up the memory chip involves setting row data at a certain time and then, two clock cycles later, the column data is set. It is not admitting that there are two clock cycles latency between a read data operation and a write data operation." on Brief page 9, line 15 through page 10, line 2, the Examiner respectfully disagrees.

In fact, the Appellant merely alleges that the Appellant is not stating a 2 clock cycles latency between a read data operation and a write data operation. However, in contrary to the Appellant's statement, the specification clearly shows said 2 clock cycles latency between said read data operation and said write data operation in Fig. 2 and Application, page 4, lines 23-24.

Moreover, the Appellant fails to explain how to substantially simultaneously transferring data to at least two destination with separate operation signals, i.e., read at T4/5 and write at T7 operations in Fig. 2.

Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

In response to the Appellant's argument with respect to "2. Claims 10 and 11 are definite. While it is clear that 10 and 11 had typographical errors in them, applicant had attempted to corrected ..." on Brief page 10, lines 3-12, the Examiner agrees.

In fact, the after final amendment has not been entered because it raised new issues and newly added claims, and thus the claims 10 and 11 rejection under 35 U.S.C. 112, second paragraph (indefiniteness) have been maintained.

However, the Examiner assumed the term "said FIFO device" as --said FIFO data source-- for the claim rejection based on prior art, i.e., the alleged typographical error was corrected before the claim rejection was performed.

In response to the Appellant's argument with respect to "3, 4 and 5. Claims 1-19 are patentable over Applicant Admitted Prior Art in view of Masterson et al. (U.S. 5,073,851) (claims 1, 4-8, 12, 14-16 and 19), and further in view of DeSouza (claims 2, 3, 9-11 and 13) and further in view of IBM_TDB December 1979, vol. 22, Issue No. 7, pages 2651-2654 (claims 17 and 18). ... Thus, the prior art is not at all doing what applicant is doing. The prior art is not transferring a unit of data to at least two destinations substantially simultaneously by supplying the data from the source to a first destination as a read operation and to a second destination as a write operation. ... Claim 1 discusses, removing some of the details in order to illustrate applicant's point, transferring a unit of data, which includes supplying said unit of data to a first destination and supplying said unit of data to a second destination. In making the rejection, the Examiner has instead converted this to be transferring a first data to device #1 and transferring a second data to device #2. But that is not what applicant claims. ..." on Brief page 10, line 13 through page 15, line 6, the Examiner believes that the Appellant misunderstands the Examiner's claim rejection.

The Appellant essentially argues that the prior arts of the record don't teach the above argued elements. Moreover, the Examiner converted the claimed invention for making the rejection based on prior art. However, as mentioned in the above Ground of Rejection, the Appellant's claimed invention has a scope enablement problem, which causes claims 1-19 rejection under 35 U.S.C. 112, first paragraph (scope enablement issue), and it disturbs a proper search of prior art. Therefore, the Examiner presumed the Appellant's invention in light of the specification, and converted the claimed invention being enabled in light of the specification.

All the claimed limitations of the enabled invention have been suggested by the combination of the references in the prior art of the record.

Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

In response to the Appellant's argument with respect to "Claims 2, 3, 9-11 and 13 rejected under 35 U.S.C. 5103(a) as allegedly being unpatentable over AAPA in view of Masterson and further in view of Desouza et al, U.S. 5,379,289. Applicant respectfully traverses. Desouza adds nothing that would overcome the conceptual difference between Masterson and applicant's methods and devices as noted above. Even if there were motivation to combine these documents' teachings, the resulting device and methods would still carry the above-noted difference wherein while first data is read, no data is written, and when second data is read, the first data is written, etc., requiring N+l steps for N data. This explicitly teaches away from applicant's simultaneous read/write concept. Therefore, claims 2, 3, 9-11 and 13 are submitted to be allowable." on Brief page 15, lines 7-20, the Examiner respectfully disagrees.

In fact, DeSouza teaches the claimed limitation "a source comprising a non-addressed data device", and the combination of AAPA, Masterson and DeSouza with rationale for a proper combining suggests the claimed invention.

Furthermore, as mentioned in the above Ground of Rejection, the Appellant's claimed invention has a scope enablement problem, which causes claims 1-19 rejection under 35 U.S.C. 112, first paragraph (scope enablement issue), and it disturbs a proper search of prior art. Thus, the Examiner presumed the Appellant's invention in light of the specification, and converted the claimed invention being enabled in light of the specification. The enabled invention is clearly taught by the combination of AAPA, Masterson and DeSouza, which is also shown in the above Ground of Rejection.

Therefore, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's argument with respect to " Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over AAPA in view of Masterson and further in view of IBM Technical Disclosure Bulletin, December 1979, Circuit for Tracing Branch Instructions. Applicant respectfully traverses. ..., wherein the goal is to speed operations rather than to save memory capacity. ..." on Brief page 15, line 21 through page 16, line 21, the Examiner respectfully disagrees.

The Appellant essentially argues that IBM_TDB reference relied on in a rejection is inapplicable because it does not relate to solving the same problem (i.e., the goal of the reference is not the same as the Appellant's) that appellant is addressing in its claimed invention (i.e., NOT the object of the claimed invention). The motivation to do what Appellant has done, however, does not have to be the same as the Appellant's to reach a conclusion of obviousness (See MPEP 2144). Moreover, the obviousness is not determined on the basis of purpose alone. *In re Graf,* 343 F.2d 774, 777, 145 USPQ 197, 199 (CCPA 1965). In summary, as long as there is some suggestion/motivation within the prior art to make the modification or combination, it does not have to be the same as the Appellant's.

Therefore, Appellant's argument for this point cannot be seen as persuasive.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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